CLAIMS:

1. A method of forming on a semiconductor substrate an electrostatic discharge protecting device (ESDP) together with internal circuitry to be protected by said protecting device, said method comprising the steps of:

a) forming an offset transistor arrangement in said protecting device; and

b) increasing an acceptor concentration at said offset transistor arrangement so as to selectively reduce a breakdown voltage of said offset transistor arrangement.

2. A method according to claim 1, wherein said offset transistor arrangement comprises an offset gate NMOS transistor.

3. A method according to any one of the preceding claims, further comprising the step of using a blanket ion implantation to increase said acceptor concentration.

4. A method according to claim 3, wherein said ion implantation is a p-LDD ion implantation.

5. A method according to claim 3 or 4, further comprising the step of performing photolithography and a subsequent donor ion implantation at said internal circuitry using a dose sufficient to compensate the later performed blanket acceptor ion implantation in regular NMOS transistors.

6. A method according to claim 5, wherein said preceding donor ion implantation is an n-LDD ion implantation.

7. A method according to claim 1 or 2, further comprising the step of using a p-LDD photo mask modified such that it allows to increase said acceptor concentration at said offset transistor arrangement.

8. A method according to claim 1 or 2, further comprising the step of using an additional ESD photo mask and subsequent ion implantation to increase said acceptor concentration at said offset transistor arrangement.

9. A method according to claim 8, wherein said additional ESD photo mask and subsequent ion implantation is adapted to obtain a clamping effect based on a Zener or avalanche breakdown.

10. A method according to any one of claims 1 to 3, further comprising the step of performing an additional blanket acceptor ion ESD implantation after formation of an n-LDD structure, wherein an n-LDD ion implantation dose should be high enough to compensate the blanket ESD ion implantation in regular NMOS transistors.

11. An integrated circuit arrangement comprising an electrostatic discharge protecting device (ESDP) and internal circuitry to be protected by said protecting device, wherein said protecting device comprises an offset transistor arrangement having a locally increased acceptor concentration so as to selectively reduce a breakdown voltage of said offset transistor arrangement.